REMARKS

In an Office Action mailed August 18, 2004, pending claims 1, 2, 4, 5, 7-12, 14-25 and 34-36 were examined and rejected. In response, Applicants are herein amending claims 34 and 35, and respectfully request the reconsideration and allowance of claims 1, 2, 4, 5, 7-12, 14-25 and 34-36.

In the most recent communication, Applicants again have not received a confirmation from the Examiner of consideration of an Information Disclosure Statement (IDS) submitted mailed by Certificate of Mailing on July 11, 2003. The IDS contained references BA through BG. Applicants again request consideration of these references in the next Office Action response and confirmation thereof by receipt of an initialed copy of the previously submitted substitute form for form 1449A/PTO.

Claims 35 and 36 were rejected under 35 U.S.C. 112, first paragraph. Support in claims 35 and 36 for "doping the first and second physically separated sidewall spacers with two angled implants of opposite conductivity type" was questioned. It was stated that the specification only provided support for angled implantation before the sidewall spacers are physically separated. Support for the alternative embodiment recited in claims 35 and 36 is found at page 10, lines 3-17 in connection with FIG. 12 and particularly at lines 12-15. Therein is stated "Rather than implanting at an earlier time to create first implant region 32 and third implant region 40, an alternative is to create the two implant regions at this point in the process in a directional manner as described before." Thus it is clear that support for claims 35 and 36 exists for angled implantation to occur after the first and second sidewall spacers are physically separated from each other as illustrated in FIG. 12. Accordingly, Applicants request the reconsideration and withdrawal of the rejection of claims 35 and 36 under the stated basis. Claim 35 is herein amended to correct a matter related to form only and not to the requirements of patentability. Since there is no prior art rejection of claims 35 and 36, Applicants respectfully submit that claims 35 and 36 are in condition for allowance.

Claims 1, 2, 4, 5, 7-12, 14, 16-25 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adkisson et al. (U.S. Patent 6,472,258) in view of Fried et al. (U.S. Publication 2003/0113970). It should be noted that all the rejected claims are method claims and not structure claims. Adkisson et al. teach a double gate transistor having two polysilicon gates 20 that are deposited (Col. 3, lines 30-49) in two trenches and polished. Each gate is of the same material and no doping of the gate polysilicon 20 is taught or suggested by Fried. Fried et al. teach a single gate FINFET structure having asymmetric doping. The single gate, for example, is conductive portions 26, 28 and 24 where portion 28 is counterdoped and portions 26 and 24 are oppositely doped. Because Adkisson et al. teaches a double gate transistor structure and Fried et al. teaches a single gate transistor structure having asymmetric portions, it is not logical, much less obvious, that the two references can or should be combined. Even so, combining the teachings of Fried et al. and the Adkisson et al. transistor structure does not teach or suggest how to form a dual gate transistor having two gate portions that substantially avoid counterdoping. In the Background section at page 2, lines 11-18, Applicants teach that a two-gate transistor structure having counterdoping is disadvantageous. Applicants recite in the rejected independent claims 1, 17 and 34 the physical separation of the recited oppositely doped gate regions or semiconductor portions. The recited removal step blocks migration of doping species in the resulting structure. This claim recital is not an intended use but a resulting physical characteristic of the removal step. Additionally, applying theoretical angled implant steps of opposite conductivity to the FIG. 2 structure of the Adkisson et al. transistor would result in each of the gate polysilicon 20 regions being counterdoped, especially if the angled implant occurs prior to polishing as suggested in paragraph 7 of the Office Action. At that point in the Adkisson et al. transistor structure formation, the polysilicon used to form two polysilicon gates is fully exposed above the FIG. 2 silicon nitride region and would be completely counterdoped by two directional implants of opposite conductivity type. With respect to paragraph 8 of the Office Action, the paragraph 0007 teaching of Fried fails to make obvious the rejected claims because of the counterdoping issues present in the prior art also are present in the Fried single gate structure. With respect to paragraph 9 of the Office Action, Applicants have not attacked the references individually but rather discussed what each reference teaches and how each reference differs from the present invention. Combination of Adkisson et al. and Fried et al. is not proper

as one reference is a dual gate transistor structure and the other reference is a single gate transistor structure. Nonetheless, the suggested combination does not suggest the recited methods of claims 1, 17 and 34.

In the rejection of dependent claim 9, the recited "conductive layer" was stated to be gate polysilicon 20 of the Adkisson et al. transistor. The rejection basis noted that it is not clear if Adkisson and Fried teach removing a portion of the conductive layer after performing a directional implant. Applicants submit that this point is clear. Adkisson et al. do not teach any opposite doping of the dual gates. Fried et al. do not teach the removal of any portion of the gate portions 26, 28, 24. While the combination of Adkisson et al. and Fried et al. is not logical since the transistor gate structures are double versus single, respectively, claim 9 is not suggested or made obvious by these references.

It should be noted that the discussion regarding claim 13 on page 7 of the most recent Office communication is moot in view of the prior cancellation of claim 13.

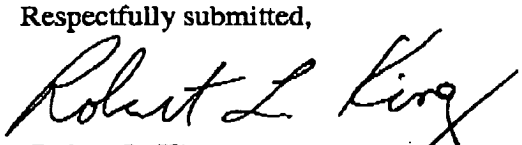
In view of the patentably distinct claim recitals of the rejected claims, Applicants respectfully request the reconsideration and withdrawal of the rejection of claims 1, 2, 4, 5, 7-12, 14, 16-25 and 34.

Claim 15 was rejected under 35 U.S.C. 103(a) as being unpatentable over Adkisson et al. (U.S. Patent 6,472,258) and Fried et al. (U.S. Pub 2003/0113970) in view of Forbes et al. (U.S. Patent 6,414,356). Forbes et al. show a dual-gated transistor structure and the patent is cited for the proposition of teaching an anneal of gate regions. Forbes et al. teach the use of an anneal to drive a deposited n+ or p+ material into underlying undoped regions at Col. 12, lines 35-55. Claim 15 is a dependent claim from claim 1 and remains distinguishable from Adkisson et al., Fried et al. and Forbes et al. for at least the reasons provided above in connection with claim 1.

Applicants therefore request the withdrawal of the rejection of claim 15.

Applicants respectfully request consideration of the amendments and the allowance of claims 1, 2, 4, 5, 7-12, 14-21, 23-25 and 34-36, thereby placing the application in condition for allowance. Should issues remain that might be subject to resolution through a telephonic interview, the Examiner is requested to telephone the undersigned at (512) 996-6839.

Respectfully submitted,



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